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Radar Waveform Generator with Fuzzy Frequency Regulation

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Abstract: Phase-locked loops (PLLs) are essential components in many modern electronic systems. Closed-loop, feedback-driven circuits generate an output signal whose frequency and phase are aligned with a given reference signal. Among the various types of PLLs, phase-detector-based designs are particularly valued for their fast response, absence of systematic phase errors, and ease of integration. In this work, we introduce a solution tailored for radar applications: the Frequency-Controlled Fuzzy Phase-Locked Loop (FPLL), by incorporates fuzzy logic into the conventional PLL architecture, enhancing system performance in environments that require rapid response and high precision. 51 frequency channels were generated by the Phase-Locked Loop. These frequency channels range from 1250 to 1350 MHz, and there is a spacing of 2 MHz between each frequency. The results showed the findings demonstrate that the fuzzy logic controller exhibits a greater overshoot compared to the proportional controller and has a more rapid response, with anticipated enhanced overall stability, resilience, and control efficacy.

Keywords: Phase-Locked Loop; radar; multi-channel radar; Fuzzy Frequency

1. Introduction

On-chip oscillators are crucial components in modern integrated circuits (ICs) and systems-on-chip (SoCs) due to their ability to generate a stable, repetitive clock signal directly within the chip. This integration offers several significant advantages and plays a vital role in the functionality and efficiency of electronic devices. While High-Resolution Phase-Locked Loop (PLL) Capabilities in Radar provide: High resolution (in range, velocity, and angle): Improving Target Discrimination, provides centimeter-level range resolution for Ultra-wideband (UWB) radar, High-resolution spectrum analysis detects and classifies low-probability-of-intercept (LPI) radars, and Cognitive radar adapts waveform dynamically to evade jamming. And 5G and mm Wave Radar Integration Millimeter-wave (mm Wave) radars [1][2][3]. However, environmental factors such as ambient temperature variations and supply voltage fluctuations, on-chip oscillators are susceptible to phase drift over time. To address this issue and maintain frequency stability, two widely used techniques are employed to align the oscillator's phase with a reference clock: Phase-Locked Loops (PLLs) and injection locking [4]. Waveform generators employ phase-locked loops (PLLs) to synthesize radar waveforms for use in surveillance [5]. When designing a PLL, it is important to keep noise, jitter, and lock time in mind [6]. Even in cases with small loop bandwidths and large beginning frequency offsets, the acquisition may be improved by combining the typical phase detector with two readily implementable frequency detectors [7]. Therefore, this topic has taken on great importance from researchers with the aim of Using a numerical simulation tool to examine the importance of multi-channel to improve: the Spatial Resolution & Beamforming, steering beams electronically for the multiple antennas in Phased-array radars, the angular resolution in MIMO (Multiple-Input Multi-ple-Output) Radar, enhances moving target detection in clutter (e.g., airborne radar) [8], [9]. Therefore, we are exposed in our study to a multi-channel, high-resolution, rapid locking mechanism designed to achieve fast lock times throughout the locking procedure, all the while enhancing jitter performance, and compare the results with other filters.

The Phase-Locked Loop (PLL) is a well-liked technique for tracking the frequency and phase of an input signal; it uses feedback to improve its signal estimation continuously. A generic PLL architecture is shown in Figure 1.

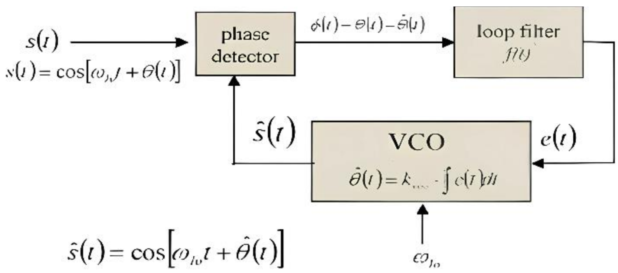


Figure 1: Standard Phase-Locked-Loop Design

Phase locking generally employs the three component actions shown below in a generic format:

Phase-error generation, or "phase detection," is a process that identifies the phase discrepancy between the received signal's phase, θ(t), and the receiver's estimation of this phase, θ (t). The authentic signals are [10],

$$s(t) = \cos(\omega_{to} + \theta(t)) \quad (1)$$

and

$$\hat{s}(t) = \cos(\omega_{to} + \hat{\theta}(t)) \quad (2)$$

For synchronization purposes, however, only their phase difference is significant. The phase error is a common term for this discrepancy.

$$\phi(t) = \theta(t) - \hat{\theta}(t). \quad (3)$$

Often referred to as "loop filtering," phase-error processing uses averaging to identify fundamental phase difference patterns from the phase error. Phase-error processing often eliminates irrelevant components from the phase error signal, such as random noise. Any gain that is created by the phase detector is reduced by the loop filter.

Reconstructing the local phase using the processed phase error is an analog technique that aims to align the incoming phase. This method is called a "voltage-controlled oscillator" (VCO), θ(t). The phase reconstruction aims to enforce $\phi(t) = 0$ by generating a local phase $\hat{\theta}(t)$ to ensure that s(t) aligns with s(t) [11]. Each phase-locking system requires a certain duration to project the incoming phase, assess the precision of that projection, and generate a new phase error. The phase-lock system (FPLL) exhibits increased susceptibility to anomalies and random noise as the speed of phase deviation detection escalates. Consequently, in the design of a synchronization system, the communication engineer must judiciously balance these two conflicting impacts. The complexity of this trade-off may vary based on the architecture of the input signals [12]. Without incorporating pilot or control signals in the input signal, one may only estimate the frequency of the sent signal or directly evaluate the phase inaccuracy.

$$H_{lp}(S) = K_{lp}F_{lp}(S) \quad (4)$$

K_{LP}= 1 for passive filters and may be much bigger than 1 for active filters. One popular way to represent the closed-loop transfer function of a PLL is from the theory of feedback control systems:

$$H(S) = \frac{K_d H_{lp}(S) K_o}{S + K_d H_{lp}(S) K_o / N} \quad (5)$$

The phase detector's feedback input to the voltage-controlled oscillator's (VCO) output is represented by N. After a charge pump is implemented, a phase frequency detector is added to the system. The Integral Fuzzy System, a mathematical method for addressing uncertainty, was developed by Lotfi Zadeh in 1965. The concept of word processing is based on the soft computing connection it establishes[13]. It offers a method for addressing uncertainty. Fuzzy theory provides a way to convey phrases like "many," "low," "medium," "often," and "few" in language. Fuzzy logic often offers a framework for inference that aligns with rational human thinking capabilities. Approximate reasoning is well-suited for fuzzy logic systems. Fuzzy logic systems provide reduced control complexity and more rapid, seamless responses compared to standard systems [14]. The essential elements of a Fuzzy system are shown in Figure 2.
Fuzzy systems depend on four primary components: an inference engine, a repository of fuzzy rules, a defuzzifier, and a fuzzyifier. When exact mathematical formulations are unfeasible, fuzzy logic controllers (FLCs) provide a viable alternative [15]. Supplementary advantages comprise:

- It can operate with less accurate inputs. • It does not require high-speed processors.
- It exhibits greater robustness compared to alternative nonlinear controllers.

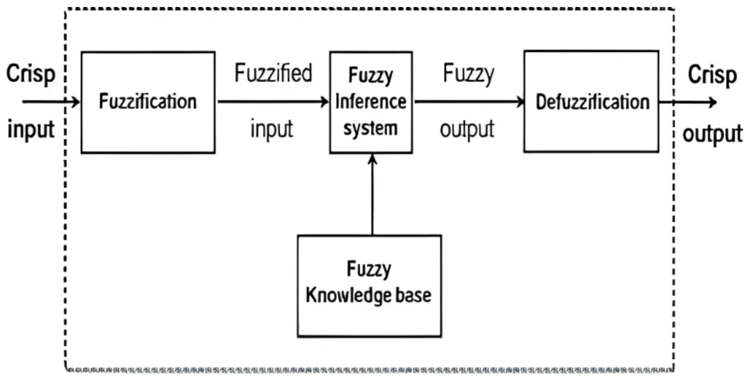


Figure 2: simple fuzzy system

2. The Architecture of the Proposed FPLL

51 frequency channels are generated by the proposed FPLL. These frequency channels range from 1250 to 1350 MHz, and there is a spacing of 2 MHz between each frequency. The total design of the proposed FPLL is illustrated in Figure 3, which can be found here. The synthesized frequency is divided into 51 channels by splitting it between 625 and 675, which results in the production of a signal with a frequency of 20 MHz. This signal is then compared to a reference signal with the same frequency using an XOR operation. A filter with a cutoff frequency of one hundred kilohertz will be applied to the erroneous signal that was produced by the comparator

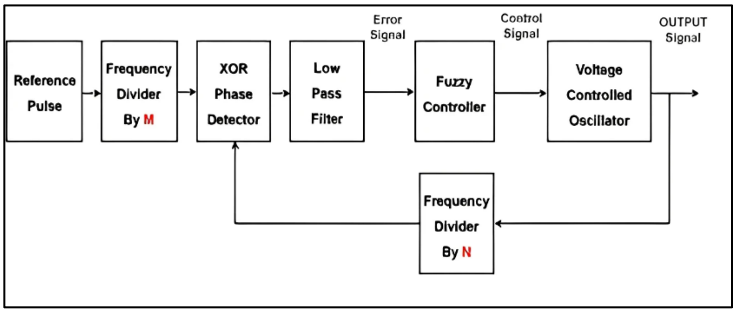
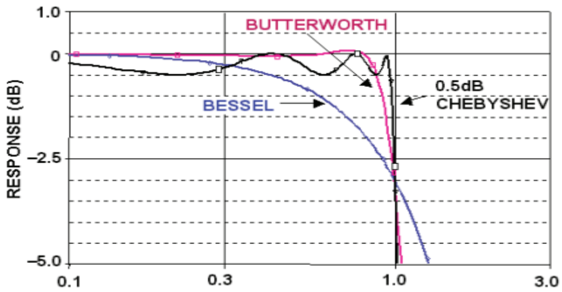


Figure 3: The proposed FPLL system

The ideal trade-off between phase response and attenuation is found in the Butterworth filter. Because it lacks ripple in either the pass or stop bands, as illustrated in figure (4), it is occasionally designated as a maximally



flat filter.

Figure 4: Evaluate the Bessel, Butterworth, and Chebyshev Filters' Amplitude Responses in Comparison

3. Results and Discussion

Simulink, a MATLAB tool, is used to simulate the proposed FPLL architecture. The block diagram of the simulation is shown in Figure 5. Afterwards, we assess how well the suggested approach works. In this case, we'll change N from 625 to 675 and assume that the frequency channels change dynamically between channels 1 and 51.

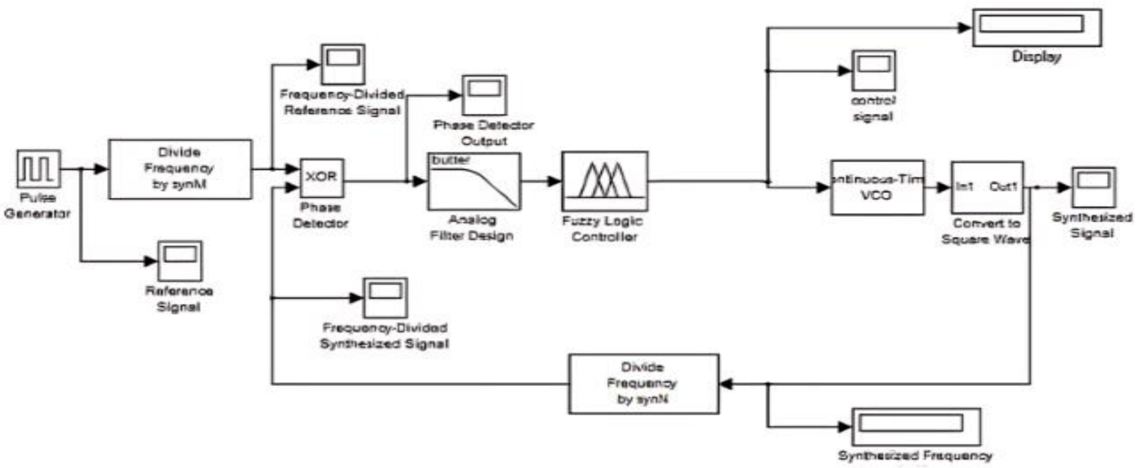


Figure 5: The simulation block diagram

An object's membership value in the fuzzy set is specified by a function that transfers it from the domain of interest to the set. This function is referred to as a membership function. In Figures 6 and 7, we can see the membership functions representing the chosen input (the value of the error signal, which may be anywhere from 0 to 1) and the control action valve, which can be anywhere from 0 to 11. For the calculation to be reasonably easy, the study employs the triangular form [15].

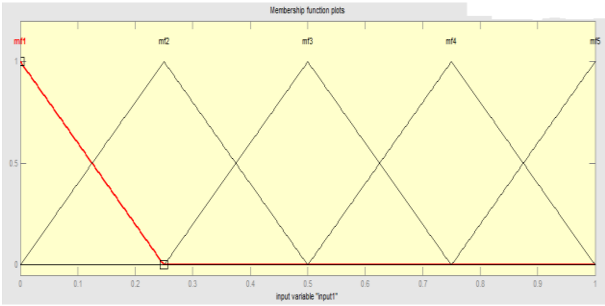


Figure 6: Input Membership function

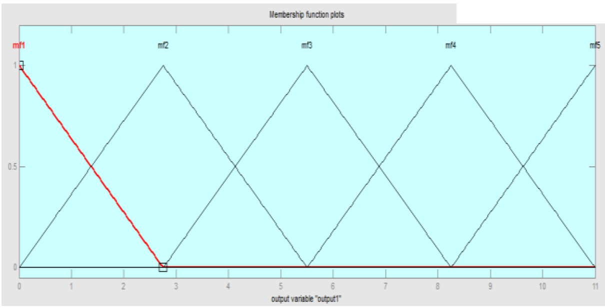


Figure 7: Output Membership function

Figures (8), (9) show the Surface viewer of the fuzzy system and the Rule Viewer for the Fuzzy controller, consequently.

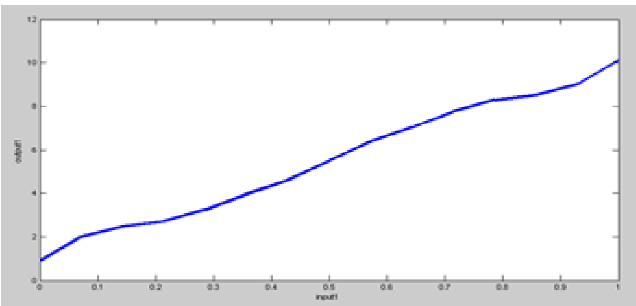


Figure 8: Surface viewer

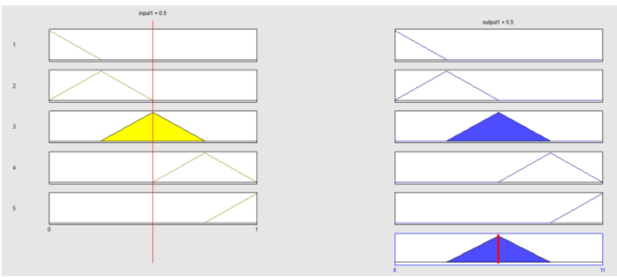


Figure 9: Rule Viewer

For a proportional controller, the values of the input and output ranges are ascertained from the experimental measurement. Fuzzification methods primarily include Mamdani and Sugeno, while Defuzzification methods are most commonly used in [16]:

- Adaptive integration,
- Centroid,
- Center of mass,
- Fuzzy clustering defuzzification,
- First of maximum,
- Last of maximum,
- Mean of maxima,
- Semi-linear defuzzification
- Centroid approach.

Figures (10), (11), and (12) show the graphs of the traditional proportional and fuzzy logic controllers, facilitating their comparison. The findings demonstrate that the fuzzy logic controller exhibits a greater overshoot compared to the proportional controller and has a more rapid response; the proportional controller reaches the same value of fuzzy after nearly 1.4 x 10^{-5} sec. While figures (11) and (12) demonstrate the superiority of fuzzy over proportional in channels 26 and 51, respectively, the two figures show that proportional up to the same value as fuzzy after 1 x 10^{-5} sec. In every case, the lock time is almost the same for both controllers. The results prove the advantages of a proportional controller in comparison to a fuzzy controller. Anticipate enhanced overall stability, resilience, and control efficacy. Proportional controllers are characterized by expedited reaction times, reduced overshoot, and enhanced stability.

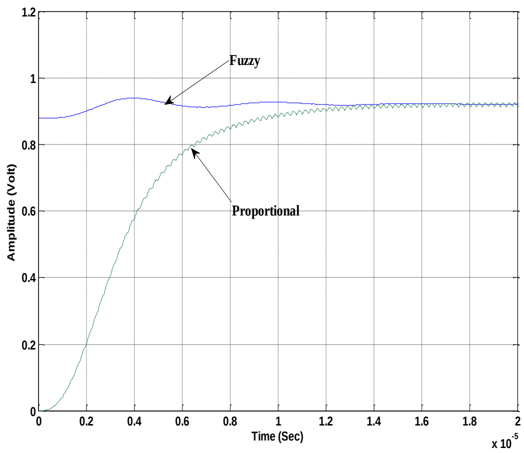


Figure 10: Response of the system when using FLC& Proportional controllers for channel No.6

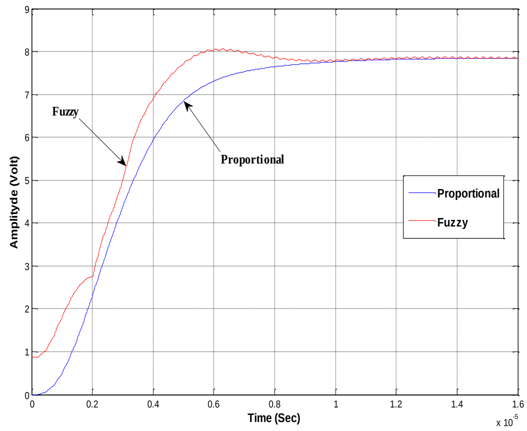


Figure 11: Response of the system when using FLC& Proportional controllers for channel No.26

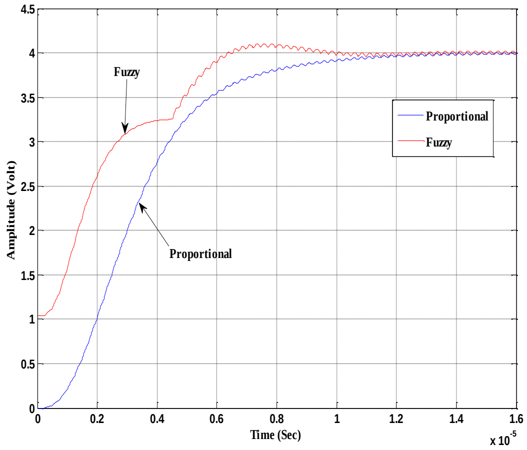


Figure 12: Response of the system when using FLC& Proportional controllers for channel No.51

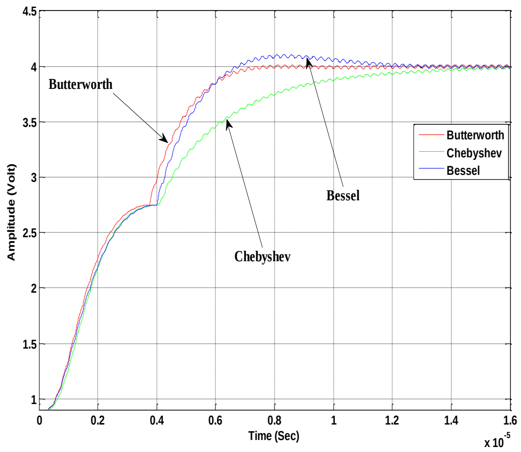


Figure 13: Comparison of control action

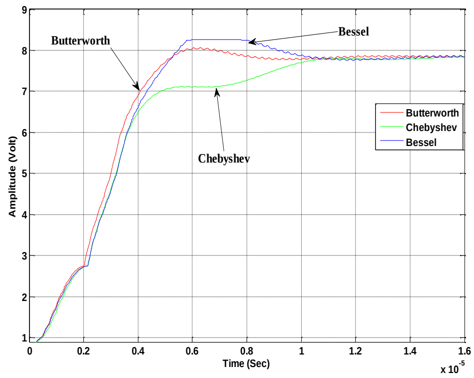


Figure 14: Comparison of control action

Figures (13) and (14) show the control action responses of the developed system for channels (1300, 1350 MHz). The sequence of their employment is as follows: Butterworth, Chebyshev, and Bessel filters. Because it produces the smallest values for lock time, overshoot, and settling time, the Butterworth filter is ideal for this application.

Figure (15) shows the system's response generation for the first five channels (channels 1–5) using the Fuzzy Logic controller.

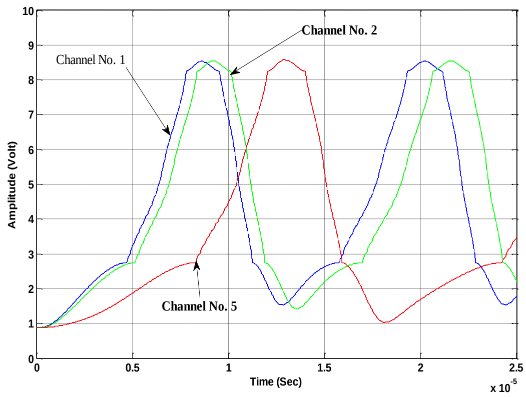


Figure 15: Response of the system when using FLC for the first 5 channels

The figure indicates that the fuzzy controller fails to achieve the target frequency output for the first five channels, but the proportional controller effectively locks all channels over the frequency range of 1250 MHz to 1350 MHz. These findings indicate that fuzzy logic alone is inadequate for generating valuable outcomes and that the parameters of the membership function are poorly assessed. Consequently, we recommend using the appropriate method to ascertain the parameters of the membership functions.

4. Conclusions

This work presents a thorough design solution for a multi-channel, high-resolution Fuzzy Frequency Control Phase-Locked Loop (FPLL) intended for Radar Waveform Synthesis in surveillance radar systems, which employs a Fuzzy Logic Controller. This allows for faster lock times while improving jitter performance in the lock. To determine the best filter for the FPLL system, the responses of many all-pole filters, including the Bessel, Butterworth, and Chebyshev filters, are compared. The results show that the Butterworth filter is the best option for this strategy. Furthermore, the data indicate that the estimation of the membership function parameters is inadequate, and relying solely on fuzzy logic yields unsatisfactory results. As a result, to obtain the parameters of the membership functions, we recommend utilizing the proper techniques.

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